

WHAT IS CLAIMED IS:

1 1. A method comprising:
 2 describing a representation of a first simulation model
 3 to a graphical user interface using hardware descriptions
 4 stored in a database;
 5 receiving a response of the first simulation model to a
 6 first signal applied to the model; and
 7 subsequently describing a second simulation model to the
 8 same graphical user interface.

1 2. The method of claim 1 further comprising receiving a
 2 response of the second simulation model to a second signal
 3 applied to the model.

1 3. The method of claim 2 wherein describing a second
 2 simulator model includes changing the hardware descriptions
 3 stored in the database.

1 4. The method of claim 1 wherein the simulation model
 2 represents a processor chip.

20241223-010702

1 5. A method comprising:
 2 causing functional processes to be associated with
 3 respective hardware descriptions stored in a database;
 4 causing the functional processes to be implemented in a
 5 simulation model;
 6 associating graphical user interface instructions with
 7 the hardware descriptions; and
 8 causing the instructions to be used to simulate a chip
 9 design response on the graphical user interface.

1 6. The method of claim 5 including describing coupling of
 2 the functional processes in a first level of hierarchical
 3 relationships.

1 7. The method of claim 6 including causing the first level
 2 hierarchical relationships to be combined into a second level
 3 of hierarchical relationships.

1 8. The method of claim 7 further comprising repeatedly
 2 causing the combining of hierarchical relationships until the
 3 chip design is described.

1 9. The method of claim 5 wherein describing a second
 2 simulator model includes changing the hardware descriptions
 3 stored in the database.

10041753-010702

1 10. The method of claim 5 wherein the chip design represents
2 a processor chip.

1 11. An apparatus comprising:

2 a processor coupled to a memory storing instructions that
3 cause the processor to:

4 associate functional processes with respective
5 hardware descriptions stored in a database;

6 execute the functional processes in a simulation
7 modeler;

8 associate graphical user interface instructions with
9 the hardware descriptions; and

10 use the instructions to simulate a chip design
11 response on a graphical user interface.

1 12. The apparatus of claim 11 wherein the hardware
2 descriptions describe a coupling of the functional processes
3 in a first level of hierarchical relationships.

1 13. The apparatus of claim 12 wherein the first level
2 hierarchical relationships are combined into a second level of
3 hierarchical relationships.

1 14. The apparatus of claim 13 wherein hierarchical
2 relationships are repeatedly combined until the chip design is
3 described.

1004-1753-010702

1 15. The apparatus of claim 11 wherein the processor is
2 configured to change the simulation model in response to a
3 change in the hardware descriptions stored in the database.

1 16. The apparatus of claim 11 wherein the chip design
2 represents a processor chip.

1 17. An article comprising a computer-readable medium storing
2 computer-executable instructions for causing a computer system
3 to:

4 associate functional processes with respective hardware
5 descriptions stored in a database;
6 implement the functional processes in a simulation model;
7 associate graphical user interface instructions with the
8 hardware descriptions; and
9 use the instructions to simulate a chip design response
10 on the graphical user interface.

1 18. The article of claim 17 wherein the hardware descriptions
2 describe a coupling of the functional processes in a first
3 level of hierarchical relationships.

1 19. The article of claim 18 wherein the first level
2 hierarchical relationships are combined into a second level of
3 hierarchical relationships.

20201001 010702

1 20. The article of claim 19 wherein hierarchical
2 relationships are repeatedly combined until the chip design is
3 described.

1 21. The article of claim 17 wherein the computer system is
2 configured to change the simulation model in response to a
3 change in the hardware descriptions stored in the database.

1 22. The article of claim 17 wherein the chip design
2 represents a processor chip.

20200705 10441753